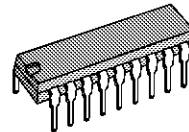


## SMART CARD INTERFACE

ADVANCE DATA

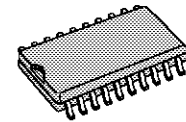
- 8 DIFFERENT VPP OUTPUT VOLTAGE LEVELS
- V<sub>PP</sub>, V<sub>CS</sub> RISE AND FALL TIME FULL SPEC WITH ISO/IEC 7816-3
- POWER SUPPLY OUTPUT FOR MEMORY CARD (5V/80mA)
- POWER ON/OFF RESET
- AUTOMATIC SWITCH-OFF OF ALL FUNCTIONS IF THE REGULAR OPERATION IS ABORTED BY EXTRACTING THE SMART CARD
- INTERNAL STATUS FAILURE CODING
  - INSERTION FAILURE CODE
  - OVERTEMPERATURE FAILURE
- ANTI-BOUNCING SYSTEM
- INPUT/OUTPUT LOGIC TTL COMPATIBLE
- THERMAL PROTECTION

### MULTIPOWER BCD TECHNOLOGY



Powerdip 12+3+3

L6605



SO 12+4+4

L6605D

#### ORDERING NUMBERS:

supply the card and V<sub>PP</sub>/50mA to write the memory inside the card; the V<sub>PP</sub> voltage can be programmed by means of the 3 serial input bit (see TAB, 1).

**Table 1: 3 bit DAC CODE**

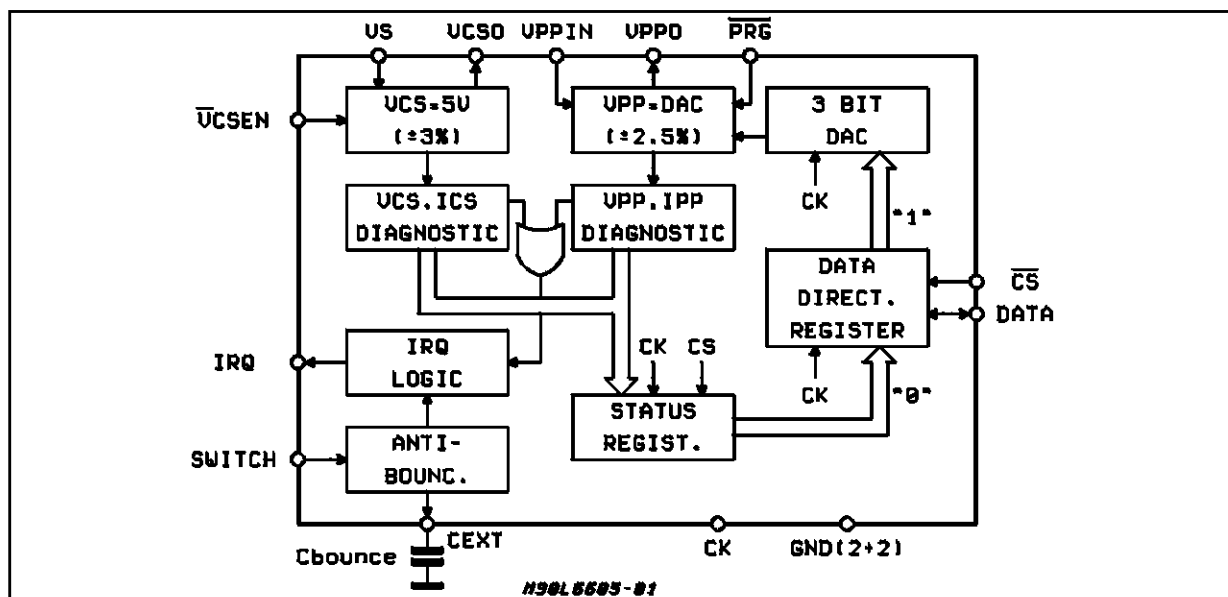
CODE	V <sub>PP</sub>
0 0 0	5V
0 0 1	10V
0 1 0	12.5V
0 1 1	13.5V
1 0 0	15V
1 0 1	18V
1 1 0	21V
1 1 1	25V

### DESCRIPTION

The L6605 is an IC dedicated as intelligent interface between different types of smart cards and microprocessors. The internal architecture can be shared in a power supply section and in a diagnostic parts.

The power supply section can deliver 5V/80mA to

### BLOCK DIAGRAM



## L6605

### DESCRIPTION (continued)

The diagnostic part allows to monitor failures due to overtemperature or wrong card positioning. The failures are internally coded and readable inside the STATUS REGISTER through the bidirectional pin DATA configured in output.

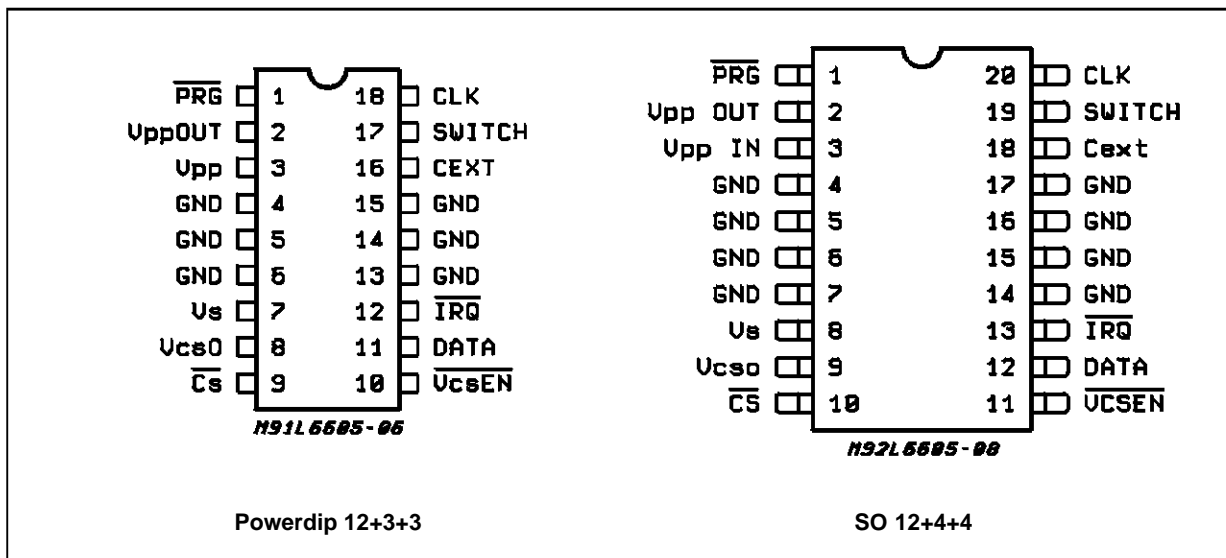
The antibouncing circuitry, active during card insertion only, rejects repetitive switching-on of the power supply sections.

The antibouncing circuitry, active during card insertion only, rejects repetitive switching-on of the power supply sections.

### PIN FUNCTION

Pin	Description
V <sub>S</sub>	Input Power Supply voltage for V <sub>CS</sub> regulated output and for device supply.
V <sub>CSO</sub>	Output regulated voltage for card supply; I <sub>CSmax</sub> = 80mA; overload protected (81 to 200mA)
V <sub>PPIN</sub>	Input power supply for V <sub>PP</sub> regulated voltage
V <sub>PPOUT</sub>	Programmable output regulated voltage for memory card writing; 8 voltage levels are allowed by means of 3 bit DAC. I <sub>PPmax</sub> = 50mA.
$\overline{V_{CSEN}}$	(Active Low) V <sub>CS</sub> supply input enable; Its value is fixed from the $\mu$ P allowing or not the normal R/W operations on the card.
SWITCH	Input signal produced by the reader system indicating that a card has been inserted. Internally, an antibouncing system is provided to avoid multiple switching.
$\overline{CS}$	Chip select (active low). $\overline{CS}$ low level indicates an I/O operation request from $\mu$ P.
IRQ	Interrupt Request (Active low). An IRQ low level indicates that a card insertion/extraction or Failure has occurred.
$\overline{PRG}$	Program (Active low). $\overline{PRG}$ low level enables L6605 to deliver in output the V <sub>PP0</sub> level set by 3 bit DAC.
DATA	I/O pin for data exchange between $\mu$ P and the device. Through this pin flow 3 bit input DAC or 2 bit STATUS REGISTER code.
CK	External clock.
C <sub>EXT</sub>	Pin to connect an external capacitor for antibouncing delay time.
GND	4 pins to ground.

### PIN CONNECTIONS (Top view)



### THERMAL DATA

Symbol	Parameter	L6605	L6605D	Unit
R <sub>thj-amb</sub>	Thermal Resistance Junction to Ambient	60	50 (*)	°C/W

(\*) Soldered on a 35 $\mu$  thick 6cm<sup>2</sup> P.C. board copper area.

**ELECTRICAL CHARACTERISTICS** ( $V_S = 12V$ ;  $T_j = 25^\circ C$ )

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_S$	Supply Voltage		10	12	15	V
$V_{CS}$	Card Supply Voltage (Logic Inputs onset)	$I_{CS} = 80mA$ , $V_S = 12V$	4.85	5	5.15	V
		$I_{CS} = 1mA$ to $80mA$ $V_S = 10V$ to $15V$ $C_{LOADmin} = 5nF$ ; $C_{LOADmax} = 20\mu F$	4.75	5	5.25	V
$I_{CS}$	Current Supply Card				80	mA
$I_{CSS}$	$I_{CS}$ Short Circuit	$V_S = 12V$	81		200	mA
$V_{PPI}$	$V_{PP}$ Supply Voltage		$V_{PPO} + 2.5V$		33	V
$V_{PPO}$	Programming Voltage	$I_{PP} = 50mA$ ; $V_{PPI} = 30V$ ; $T_{on} \leq 5ms$	-2.5%	$V_{DAC}$	+2.5%	V
		$I_{PP} = 1mA$ to $50mA$ $V_{PPI} = \text{max. } 33V$ (see note 1) $C_{LOADmin} = 5nF$ $C_{LOADmax} = 500nF$ (see note 2)	-5%	$V_{DAC}$	+5%	V
$I_{PP}$	Output Program. Current	$V_{PPI} = 30V$			50	mA
$I_{PPS}$	$I_{PP}$ Short Circuit		51		150	mA
$t_{on}$	$V_{PP}$ , Rise Time	$C_{LOADmin} = 5nF$ $C_{LOADmax} = 500nF$ (see note 2) $I_L = 50mA$ (see note 1)			200	$\mu s$
$t_{off}$	$V_{PP}$ , Fall Time				200	$\mu s$
$t_{shadow}$	Shadow Timing	$C_{bounce} = 0.1\mu F$		1		ms
$V_{SWLOW}$	Low Level Switch Input				0.8	V
$V_{SWHIGH}$	High Level Switch Input		2		$V_S - 2V$	V
$t_{CKON}$	Clock ON Time	$C_{LOAD} = 50pF$ , $I_{SINK} = 4mA$ , $V_L = 0.4V$	1			$\mu s$
$t_{CKOFF}$	Clock OFF Time		1			$\mu s$
$t_D$	Delay Time		250			ns
$t_{SET-UP1}$	1st bit Set-up Time		500			ns
$t_{HOLD1}$	1st bit Hold Time		500		$t_{CKON}$	ns
$t_{SET-UP2}$	Data Set-up Time		500			ns
$t_{HOLD2}$	Data Hold Time		500			ns
$t_{SCK}$	Clock Set-up Time		250			ns
$t_{HCK}$	Clock Hold Time	250			ns	
$f$	Clock Frequency				500	KHz
SR	$V_{PP}$ Slew Rate	From rest state to programming state and viceversa			2	$V/\mu s$
$V_{STH}$	Power ON/OFF Threshold	Logic inputs onset		8.5	9.5	V
$V_{SHY}$	$V_{STH}$ Hysteresis			0.6		V
$T_S$	Thermal Shutdown			180		$^\circ C$
$T_H$	Thermal Hysteresis			20		$^\circ C$

**Note 1:** True for values in Tab. 1 only. ; **Note 2:** Values higher than 500nF are permitted, but the ton, toff timing will be out ISO norm.

**CIRCUIT OPERATION****CARD POWER SUPPLY**

Regulated voltage to supply the card (5V/80mA). During nominal condition ( $V_S = 12V$ ,  $I_{CS} = 80mA$ ) the  $V_{CS}$  range variation is equal to  $\pm 3\%$ . While during line/load variation ( $V_S = 10V$  to  $15V$ ;  $I_{CS} = 1mA$  to  $80mA$ ) the  $V_{CS}$  range is  $\pm 5\%$ . An internal circuitry checks the  $I_{CS}$  level; the pro-

tection block activates an IRQ with the proper failure code when the output current is in 81mA to 200mA range.

**PROGRAMMING POWER SUPPLY**

L6605 works in step-down mode by means of the programmed output voltage  $V_{PP}$ . 8 $V_{PP}$  levels can be selected programming the 3 bit DAC as per Table 1. During nominal conditions ( $I_{PP} = 50mA$ ;  $V_{PPI} = 30V$ ) the  $V_{PP}$  range variation is equal to

## L6605

$\pm 2.5\%$ ; while during line/load variation ( $I_{PP} = 1\text{mA}$  to  $50\text{mA}$ ;  $V_{PPI} = \text{max. } 33\text{V}$ ) the  $V_{PP}$  range is  $\pm 5\%$ . An internal circuitry checks the  $I_{PP}$  level; the protection block activates an IRQ with the proper failure code when the output current is in  $51\text{mA}$  to  $150\text{mA}$  range. Under the power ON/OFF threshold value the logic section and the power supply regulators are disabled.

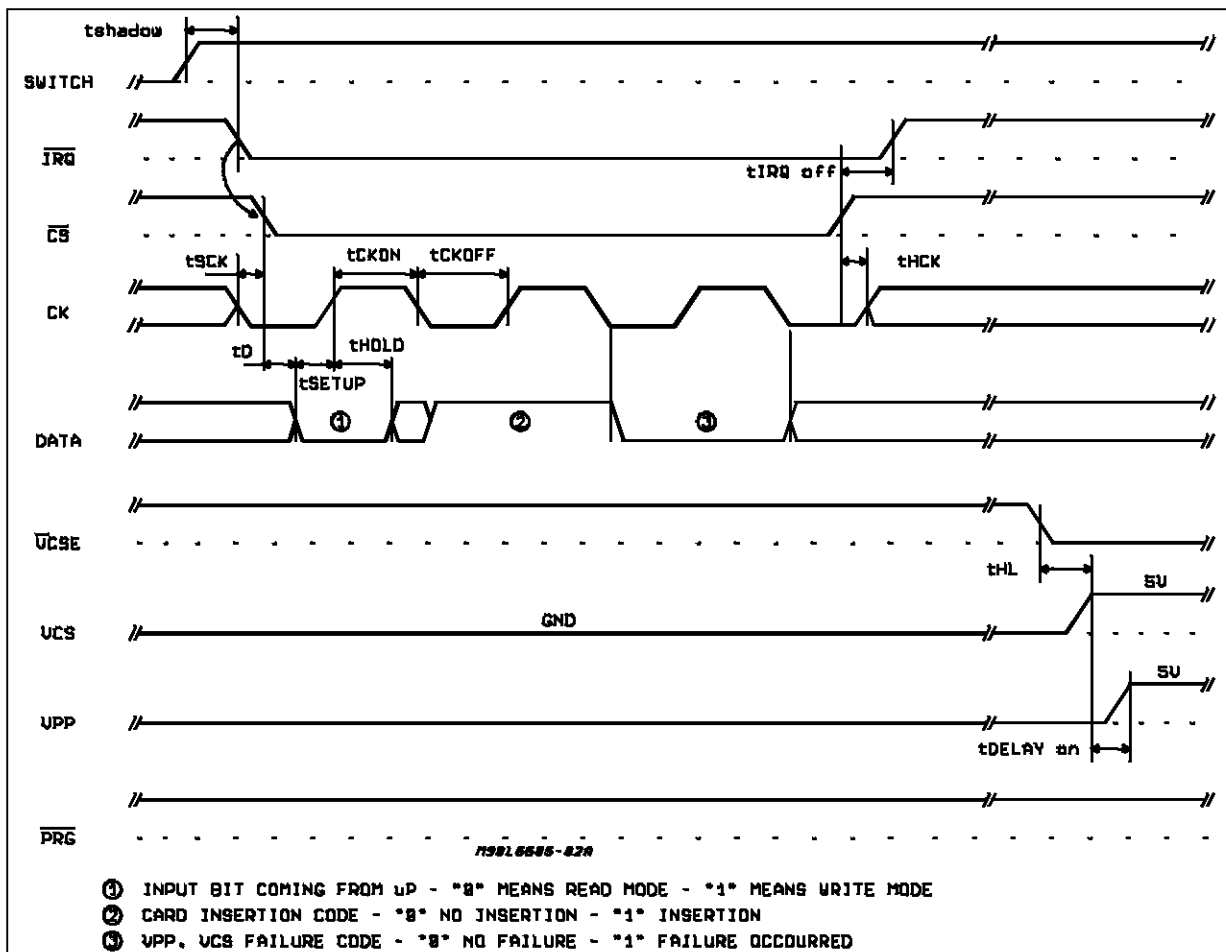
### LOGIC SECTION

L6605 includes a logic circuitry in order to protect, both card and itself. If a failure occurs an asynchronous IRQ is sent to the  $\mu\text{P}$ ; consequently the  $\mu\text{P}$  forces low CS signal as I/O request. After CS variation the  $\mu\text{P}$  sends also one "data direction bit" into DATA DIRECTION REGISTER.

- Direction bit = "0"  
Pin DATA is configured in output and the  $\mu\text{P}$  reads the 2 bit STATUS REGISTER content

Code	1st bit	2nd bit
0	No insertion	No Failure
1	Card Inserted	Failure

Figure 1: Card Insertion



Failure could be overtemperature over the 2 regulators ( $V_{PP}$ ,  $V_{CS}$ ).

- Direction bit = "1"  
Pin DATA is configured in input to allow the 3 bit DAC loading and than the programming of  $V_{PP0}$  output level voltage. (see Table 1).

During card insertion only rising edge of switch signal is detected, while during card extraction switch level is detected.

In card extraction mode if occurs a mechanical extraction switch bouncing, which causes a pulse on SWITCH input pin with duration  $t \geq 50\mu\text{s}$  the L6605 will have the 1st Status Register content equal to "0" and 1 ms  $t_{\text{shadow}}$  timing like during card insertion mode.

Bouncing on SWITCH pin with duration  $T < 50\mu\text{s}$  will be transparent in the Status Register.

Figure 2: DAC Loading and Programmed Voltage on Set

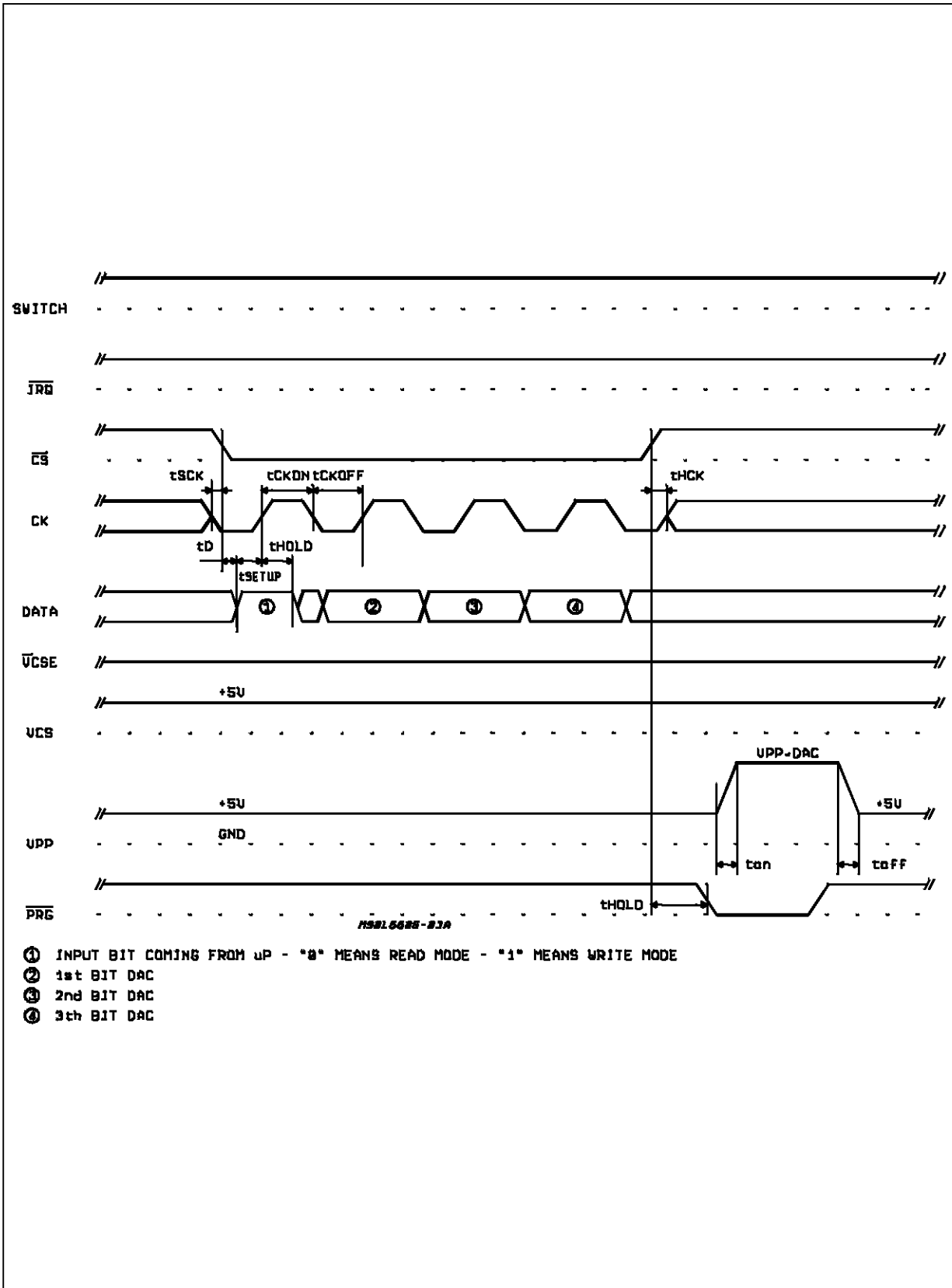


Figure 3: End Normal Operation

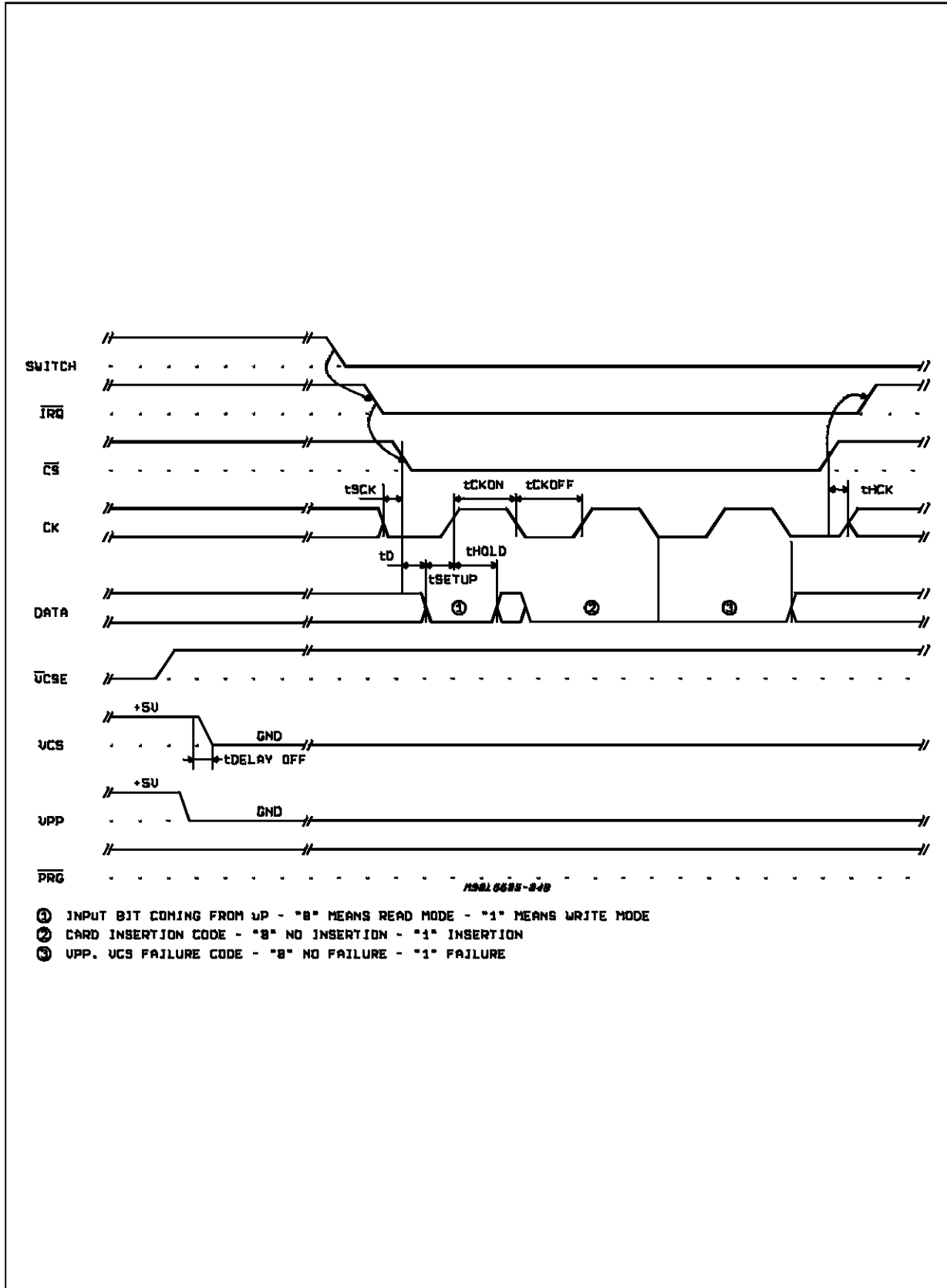


Figure 4.

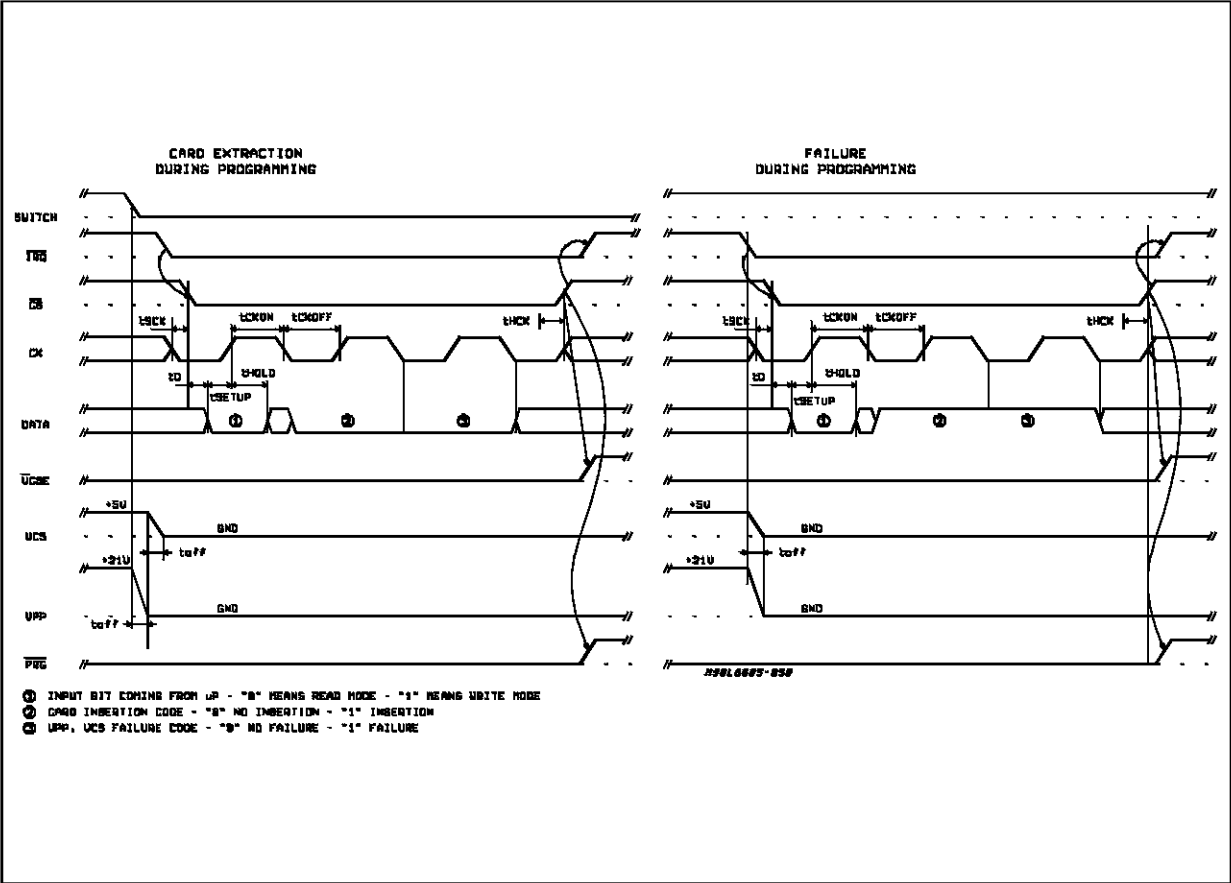
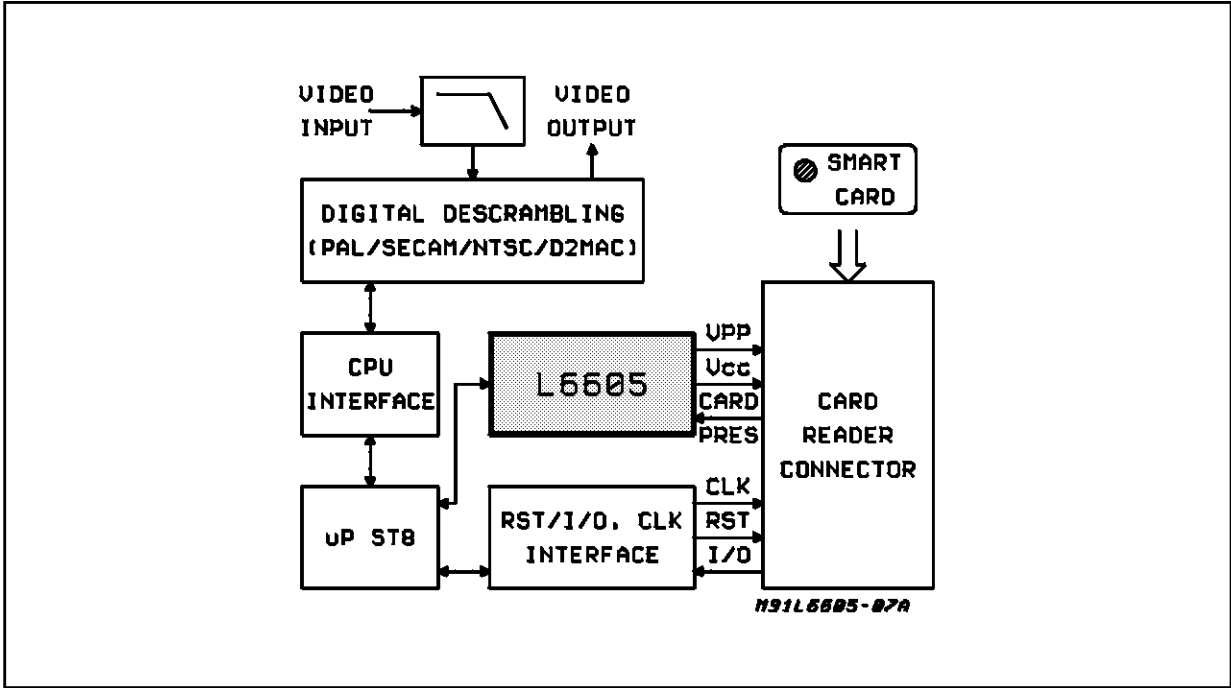
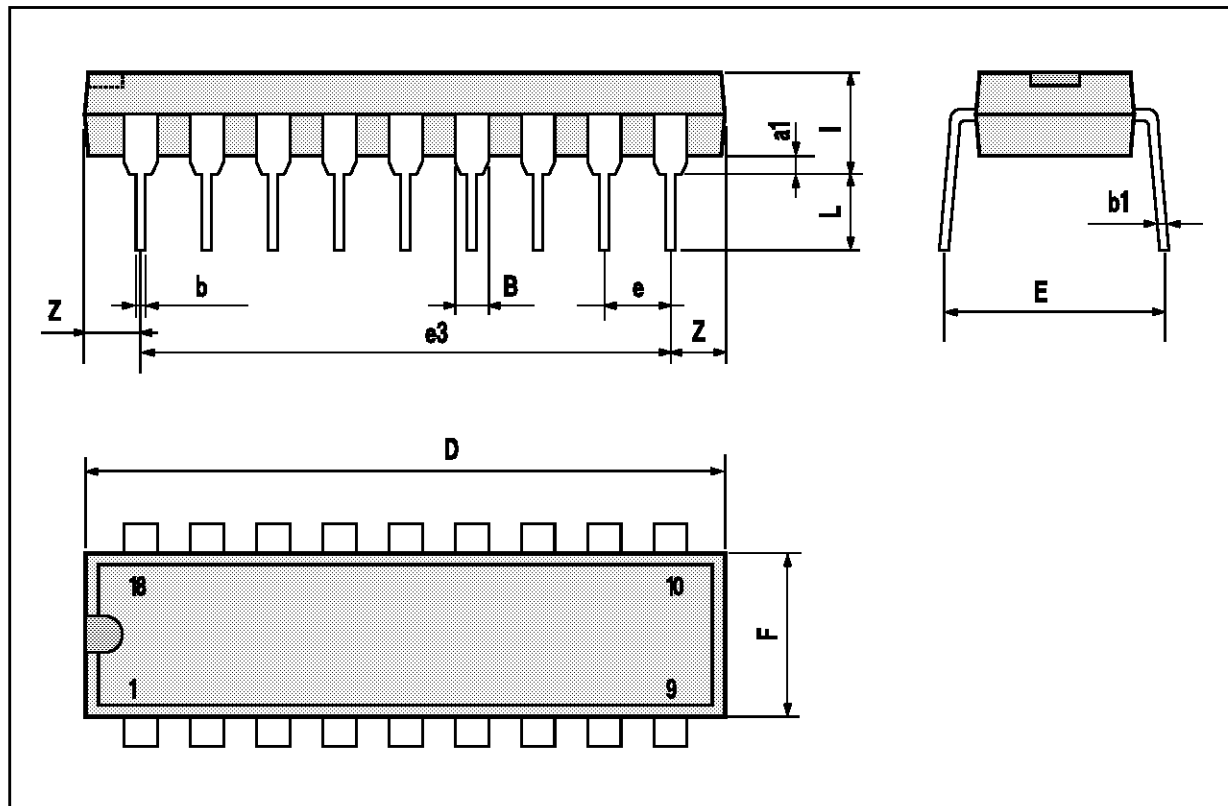


Figure 5: PAY-TV Application



## POWERDIP18 PACKAGE MECHANICAL DATA

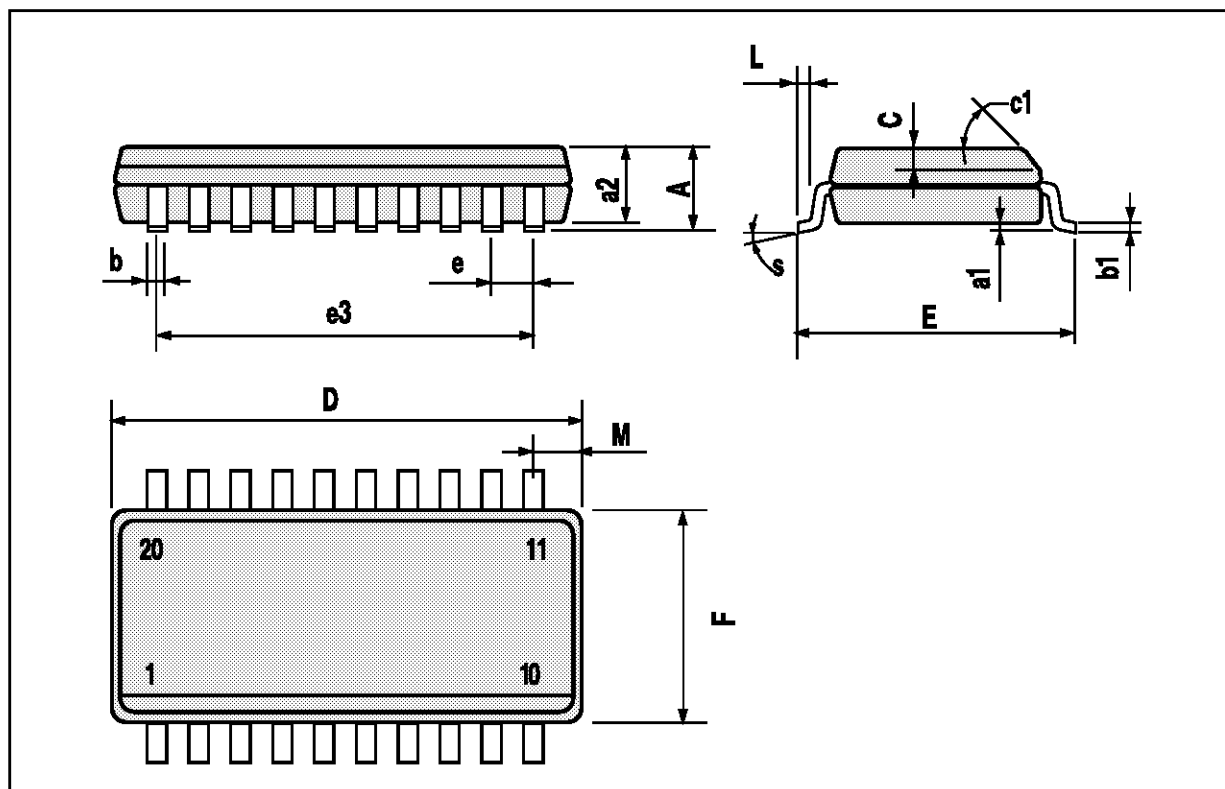
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			2.54			0.100





## SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)					



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